

CLAIMS:

add 3  
1. A method for forming graded junction regions operatively adjacent a transistor gate of CMOS circuitry, the method comprising the following steps:

providing a semiconductor material wafer;

defining a PMOS region and an NMOS region of the wafer;

providing a PMOS transistor gate over the PMOS region and providing an NMOS transistor gate over the NMOS region, the transistor gates having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gates, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

providing a masking layer over the PMOS region;

after providing the masking layer over the PMOS region, and after providing the sidewall spacers adjacent the NMOS transistor gate, implanting an n-type conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive NMOS source/drain regions within the semiconductor material operatively adjacent the NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate; and

1 after decreasing the lateral thickness of the sidewall spacers  
2 adjacent the NMOS transistor gate, implanting a p-type conductivity-  
3 enhancing dopant into the semiconductor material to form halo regions  
4 operatively adjacent the NMOS source/drain regions.

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6 2. The method of claim 1 further comprising, after providing  
7 transistor gates over the PMOS region and NMOS region, and prior to  
8 providing sidewall spacers adjacent the sidewalls of the transistor gates,  
9 forming NMOS LDD regions operatively adjacent the NMOS transistor  
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3. The method of claim 1 further comprising:

after forming the electrically conductive NMOS source/drain regions, and prior to etching the sidewall spacer material adjacent the NMOS transistor gate, stripping the masking layer from over the PMOS region;

etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate and the PMOS transistor gate, blanket implanting the p-type conductivity-enhancing dopant into the semiconductor material of both the PMOS region and the NMOS region to form halo regions operatively adjacent the NMOS transistor gate and to form PMOS LDD regions operatively adjacent the PMOS transistor gate.

4. The method of claim 3 further comprising, prior to decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate and subsequent to stripping the masking layer from over the PMOS region, forming electrically conductive PMOS source/drain regions within the semiconductor material operatively adjacent the PMOS transistor gate.

1 5. The method of claim 1 further comprising, prior to  
2 providing the masking layer over the PMOS region, forming PMOS LDD  
3 regions operatively adjacent the PMOS transistor gate.

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5 6. The method of claim 1 wherein the semiconductor material  
6 wafer comprises an overall planar global configuration, the planar global  
7 configuration establishing a virtual planar top surface and an axis  
8 normal to the virtual planar top surface, and wherein the p-type  
9 conductivity-enhancing dopant is implanted at an angle other than  
10 parallel to the axis normal to the virtual planar top surface.  
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FIG. 10

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7. The method of claim 1 further comprising:  
prior to providing the masking layer over the PMOS region,  
forming PMOS LDD regions operatively adjacent the PMOS transistor  
gate;  
after forming the electrically conductive NMOS source/drain  
regions, and prior to etching the sidewall spacer material adjacent the  
NMOS transistor gate, stripping the masking layer from over the PMOS  
region;  
etching the sidewall spacer material adjacent the PMOS transistor  
gate to decrease the lateral thickness of the sidewall spacers adjacent  
the PMOS transistor gate; and  
after decreasing the lateral thickness of the sidewall spacers  
adjacent the NMOS transistor gate and the PMOS transistor gate,  
blanket implanting the p-type conductivity-enhancing dopant into the  
semiconductor material of both the PMOS region and the NMOS region  
to form halo regions operatively adjacent the NMOS transistor gate and  
to enhance the conductivity of the PMOS LDD regions.

8. The method of claim 1 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and further comprising:

after forming the electrically conductive NMOS source/drain regions, and prior to etching the sidewall spacer material adjacent the NMOS transistor gate, stripping the masking layer from over the PMOS region;

etching the sidewall spacer material adjacent the PMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate and the PMOS transistor gate, blanket implanting the p-type conductivity-enhancing dopant at an angle other than parallel to the axis normal to the virtual planar top surface to form NMOS halo regions operatively adjacent the NMOS transistor gate and to form PMOS LDD regions operatively adjacent the PMOS transistor gate.

9. The method of claim 1 wherein the portion of spacer material removed from the sidewall spacers constitutes no more than about 90% of the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate.

10. The method of claim 1 wherein the sidewalls of the transistor gates comprise polysilicon, the method further comprising:

prior to providing sidewall spacers adjacent the sidewalls, oxidizing the polysilicon of the sidewalls.

11. The method of claim 10 further comprising, prior to providing sidewall spacers adjacent the sidewalls of the NMOS transistor gate, forming NMOS LDD regions operatively adjacent the NMOS transistor gate.

12. CMOS circuitry comprising at least one transistor formed by the method of claim 1.

FIG. 10

13. A method for forming graded junction regions operatively adjacent a transistor gate, the method comprising the following steps:

providing a semiconductor material wafer;

providing a transistor gate over the semiconductor material wafer, the transistor gate having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gate, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers, implanting a first conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive source/drain regions within the semiconductor material operatively adjacent the transistor gate;

after forming the electrically conductive source/drain regions, etching the sidewall spacer material to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers; and

after decreasing the lateral thickness of the sidewall spacers, implanting a second conductivity-enhancing dopant into the semiconductor material to form graded junction regions operatively adjacent the source/drain regions.



14. The method of claim 13 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the second conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

15. The method of claim 13 wherein the transistor is a PMOS transistor, the second conductivity-enhancing dopant is a p-type dopant, and the implant of the second conductivity-enhancing dopant forms LDD regions operatively adjacent the PMOS source/drain regions.

16. The method of claim 13 wherein the transistor is a PMOS transistor, the second conductivity-enhancing dopant is an n-type dopant, and the implant of the second conductivity-enhancing dopant forms halo regions operatively adjacent the PMOS source/drain regions.

17. The method of claim 16 wherein the second conductivity-enhancing dopant comprises phosphorus.

18. The method of claim 13 wherein the transistor is an NMOS transistor, the second conductivity-enhancing dopant is a p-type dopant, and the implant of the second conductivity-enhancing dopant forms halo regions operatively adjacent the NMOS source/drain regions.

1 19. The method of claim 18 wherein the second conductivity-  
2 enhancing dopant comprises boron.

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4 20. The method of claim 13 wherein the transistor is an NMOS  
5 transistor, the second conductivity-enhancing dopant is a n-type dopant,  
6 and the implant of the second conductivity-enhancing dopant forms LDD  
7 regions operatively adjacent the NMOS source/drain regions.

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9 21. A transistor formed by the method of claim 13.

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11 22. A method for implanting graded junction regions into a  
12 peripheral NMOS transistor and source/drain regions into a memory  
13 array of NMOS transistors, the method comprising the following steps:  
14 providing a semiconductor material wafer;  
15 defining a memory array region of the wafer;  
16 defining a PMOS region and a peripheral NMOS region of the  
17 wafer;

18 providing a PMOS transistor gate over the PMOS region, providing  
19 a peripheral NMOS transistor gate over the peripheral NMOS region,  
20 and providing an array of memory NMOS transistor gates over the  
21 memory array region, the transistor gates having opposing lateral  
22 sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gates, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

providing a masking layer over the PMOS region and over the memory array region;

after providing the masking layer over the PMOS region and the memory array region, and after providing the sidewall spacers adjacent the peripheral NMOS transistor gate, implanting an n-type conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive peripheral NMOS source/drain regions within the semiconductor material operatively adjacent the peripheral NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the peripheral NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate, implanting p-type conductivity-enhancing dopant into the semiconductor material to form halo regions operatively adjacent the peripheral NMOS source/drain regions.

1 23. The method of claim 22 further comprising, after providing  
2 transistor gates over the peripheral NMOS region and over the memory  
3 array region, and prior to providing sidewall spacers adjacent the  
4 sidewalls of the transistor gates, providing LDD regions operatively  
5 adjacent the peripheral NMOS transistor gate and providing memory  
6 gate source/drain regions operatively adjacent the memory NMOS  
7 transistor gates.

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9 24. The method of claim 22 further comprising:  
10 after forming halo regions operatively adjacent the NMOS  
11 source/drain regions, stripping the masking layer from over the PMOS  
12 region and providing a masking layer over the peripheral NMOS region;  
13 after providing the masking layer over the NMOS region, etching  
14 the sidewall spacer material adjacent the PMOS transistor gate to  
15 decrease the lateral thickness of the sidewall spacers adjacent the PMOS  
16 transistor gate; and

17 after decreasing the lateral thickness of the sidewall spacers  
18 adjacent the PMOS transistor gate, implanting n-type conductivity-  
19 enhancing dopant into the semiconductor material to form halo regions  
20 operatively adjacent the PMOS transistor gate.  
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25. The method of claim 24 further comprising, prior to decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate and subsequent to stripping the masking layer from over the PMOS region, forming electrically conductive PMOS source/drain regions within the semiconductor material operatively adjacent the PMOS transistor gate.

26. The method of claim 22 further comprising:

after forming halo regions operatively adjacent the NMOS source/drain regions, stripping the masking layer from over the PMOS region and providing a masking layer over the peripheral NMOS region;

after providing the masking layer over the NMOS region, etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate, implanting p-type conductivity-enhancing dopant into the semiconductor material to form LDD regions operatively adjacent the PMOS transistor gate.

1 27. The method of claim 26 further comprising, prior to  
2 decreasing the lateral thickness of the sidewall spacers adjacent the  
3 PMOS transistor gate and subsequent to stripping the masking layer  
4 from over the PMOS region, forming electrically conductive PMOS  
5 source/drain regions within the semiconductor material operatively  
6 adjacent the PMOS transistor gate.

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8 28. The method of claim 22 further comprising:

9 after forming the electrically conductive peripheral NMOS  
10 source/drain regions, and prior to etching the sidewall spacer material  
11 adjacent the peripheral NMOS transistor gate, stripping the masking  
12 layer from over the PMOS region;

13 etching the sidewall spacer material adjacent the PMOS transistor  
14 gate to decrease the lateral thickness of the sidewall spacers adjacent  
15 the PMOS transistor gate; and

16 after decreasing the lateral thickness of the sidewall spacers  
17 adjacent the peripheral NMOS transistor gate and the PMOS transistor  
18 gate, blanket implanting the p-type conductivity-enhancing dopant into  
19 the semiconductor material of both the PMOS region and the NMOS  
20 region to form halo regions operatively adjacent the NMOS transistor  
21 gate and to form PMOS LDD regions operatively adjacent the PMOS  
22 transistor gate.

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1           29. The method of claim 28 further comprising, prior to  
2 decreasing the lateral thickness of the sidewall spacers adjacent the  
3 PMOS transistor gate and subsequent to stripping the masking layer  
4 from over the PMOS region, forming electrically conductive PMOS  
5 source/drain regions within the semiconductor material operatively  
6 adjacent the PMOS transistor gate.

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8           30. A semiconductor wafer comprising a peripheral NMOS and  
9 a memory array formed by the method of claim 22.

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11           31. A method for forming graded junction regions operatively  
12 adjacent a transistor gate, the method comprising the following steps:

13           providing a semiconductor material wafer;

14           providing a transistor gate over the semiconductor material wafer,  
15 the transistor gate having opposing lateral sidewalls;

16           providing sidewall spacers adjacent the sidewalls of the transistor  
17 gate, the sidewall spacers having a lateral thickness and comprising a  
18 sidewall spacer material;

19           decreasing the lateral thickness of the sidewall spacers by  
20 removing only a portion of the sidewall spacers; and

21           after decreasing the lateral thickness of the sidewall spacers,  
22 implanting a conductivity-enhancing dopant into the semiconductor  
23 material to form graded junction regions operatively adjacent the  
24 transistor gate.

FOOTNOTES

1           32. The method of claim 31 wherein the semiconductor material  
2 wafer comprises an overall planar global configuration, the planar global  
3 configuration establishing a virtual planar top surface and an axis  
4 normal to the virtual planar top surface, and wherein the second  
5 conductivity-enhancing dopant is implanted at an angle other than  
6 parallel to the axis normal to the virtual planar top surface.

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8           33. The method of claim 31 further comprising, after providing  
9 the sidewall spacers and prior to decreasing the lateral thickness of the  
10 sidewall spacers, providing electrically conductive source/drain regions  
11 operatively adjacent the transistor gate.

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13           34. The method of claim 31 further comprising incorporating the  
14 transistor gate into a PMOS transistor, wherein the implanted  
15 conductivity-enhancing dopant is a p-type dopant, and wherein the  
16 formed graded junction regions are LDD regions.

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18           35. The method of claim 31 further comprising incorporating the  
19 transistor gate into a PMOS transistor, wherein the implanted  
20 conductivity-enhancing dopant is an n-type dopant, and wherein the  
21 formed graded junction regions are halo regions.



1 36. The method of claim 31 further comprising incorporating the  
2 transistor gate into an NMOS transistor, wherein the implanted  
3 conductivity-enhancing dopant is a p-type dopant, and wherein the  
4 formed graded junction regions are halo regions.

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6 37. The method of claim 31 further comprising incorporating the  
7 transistor gate into an NMOS transistor, wherein the implanted  
8 conductivity-enhancing dopant is an n-type dopant, and wherein the  
9 formed graded junction regions are LDD regions.

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11 38. A transistor formed by the method of claim 31.  
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39. A semiconductor transistor device comprising:

a region of a semiconductor material wafer;

a transistor gate over a portion of the region of the semiconductor material wafer, the transistor gate having opposing lateral sidewalls;

opposing source/drain regions operatively adjacent the transistor gate, each source/drain region having an inner lateral boundary;

opposing sidewall spacers adjacent the sidewalls of the transistor gate, each sidewall spacer having an outer lateral edge, the sidewall spacers and source/drain regions being paired such that the outer lateral edges of the sidewall spacers are displaced laterally inwardly relative to the inner lateral boundaries of the source/drain regions; and

lateral gaps, the lateral gaps extending from the outer lateral edges of the sidewall spacers to the inner lateral boundaries of the source/drain regions.

40. The device of claim 39 wherein the lateral gaps have a length, the length of the lateral gaps being from about 200 Angstroms to about 600 Angstroms.

41. The device of claim 39 further comprising graded junction regions inwardly adjacent the source/drain regions, the graded junction regions extending within the lateral gaps.

42. A method for forming a peripheral NMOS transistor and one or more memory NMOS transistors, the method comprising the following steps:

forming a peripheral NMOS transistor gate and one or more memory NMOS transistor gates;

forming source/drain regions, halo regions and LDD regions operatively adjacent the peripheral NMOS transistor gate, and forming source/drain regions operatively adjacent the one or more memory NMOS transistor gates, the steps of forming the regions occurring in a sequence such that one or more of the regions are formed last and are therefore last formed regions, wherein the LDD regions formed operatively adjacent the peripheral NMOS transistor gate are not the last formed regions; and

less than two masking layer provision steps after the formation of the LDD regions operatively adjacent the peripheral NMOS transistor gate, and prior to formation of the one or more last formed regions.

43. A method for forming graded junction regions operatively adjacent a transistor gate of CMOS circuitry, the method comprising the following steps:

providing a semiconductor material wafer;

defining a PMOS region and an NMOS region of the wafer;

providing a gate layer over the PMOS region and over the NMOS region;

1 patterning the gate layer over the NMOS region to form an  
2 NMOS transistor gate over the NMOS region while leaving the gate  
3 layer over the PMOS region unpatterned, the NMOS transistor gate  
4 having opposing lateral sidewalls;

5 providing sidewall spacers adjacent the sidewalls of the NMOS  
6 transistor gate, the sidewall spacers having a lateral thickness and  
7 comprising a sidewall spacer material;

8 after providing the sidewall spacers, forming electrically conductive  
9 NMOS source/drain regions within the semiconductor material operatively  
10 adjacent the NMOS transistor gate;

11 after forming the electrically conductive NMOS source/drain  
12 regions, etching the sidewall spacer material adjacent the NMOS  
13 transistor gate to remove only a portion of said spacer material and to  
14 thereby decrease the lateral thickness of the sidewall spacers; and

15 after decreasing the lateral thickness of the sidewall spacers  
16 adjacent the NMOS transistor gate, implanting conductivity-enhancing  
17 dopant into the semiconductor material to thereby form NMOS graded  
18 junction regions operatively adjacent the NMOS source/drain regions.

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20 44. The method of claim 43 wherein the implanted conductivity-  
21 enhancing dopant is a p-type dopant and wherein the formed NMOS  
22 graded junction regions are halo regions.  
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1           45. The method of claim 43 wherein the portion of spacer  
2 material removed from the sidewall spacers constitutes no more than  
3 about 90% of the lateral thickness of the sidewall spacers adjacent the  
4 NMOS transistor gate.

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6           46. The method of claim 43 wherein the gate layer comprises  
7 a polysilicon layer, a refractory metal layer over the polysilicon layer,  
8 an oxide layer over the refractory metal layer, and a silicon nitride  
9 layer over the oxide layer.

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11           47. The method of claim 43 further comprising, after forming  
12 the NMOS transistor gate, and prior to providing sidewall spacers,  
13 forming NMOS LDD regions operatively adjacent the NMOS transistor  
14 gate.

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16           48. The method of claim 43 wherein the opposing lateral  
17 sidewalls of the NMOS transistor gate comprise polysilicon, the method  
18 further comprising:

19           prior to providing sidewall spacers adjacent the NMOS transistor  
20 gate, oxidizing the polysilicon of the opposing lateral sidewalls to form  
21 an oxide layer along each opposing lateral sidewall.  
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1 49. The method of claim 48 further comprising, after forming  
2 the NMOS transistor gate, and prior to providing the oxide layer along  
3 each opposing lateral sidewall, forming NMOS LDD regions operatively  
4 adjacent the NMOS transistor gate.  
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6 50. The method of claim 43 wherein the semiconductor material  
7 wafer comprises an overall planar global configuration, the planar global  
8 configuration establishing a virtual planar top surface and an axis  
9 normal to the virtual planar top surface, and wherein the p-type  
10 conductivity-enhancing dopant is implanted at an angle other than  
11 parallel to the axis normal to the virtual planar top surface.  
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13 51. The method of claim 43 further comprising:  
14 after forming the NMOS transistor gate, patterning the gate layer  
15 over the PMOS region to form a PMOS transistor gate over the PMOS  
16 region.  
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52. A method for implanting graded junction regions into a peripheral NMOS transistor and into a memory array of NMOS transistors, the method comprising the following steps:

providing a semiconductor material wafer;

defining a memory array region, a PMOS region and a peripheral NMOS region of the wafer;

providing a gate layer over the PMOS, peripheral NMOS and memory array regions;

patterning the gate layer over the peripheral NMOS region to form a peripheral NMOS transistor gate over the peripheral NMOS region, the peripheral NMOS transistor gate having opposing lateral sidewalls;

patterning the gate layer over the memory array region to form an array of memory NMOS transistor gates over the memory array region, the memory NMOS transistor gates having opposing lateral sidewalls;

while patterning the gate layer over the peripheral NMOS region, and while patterning the gate layer over the memory array region, leaving the gate layer over the PMOS region unpatterned;

providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers forming electrically conductive peripheral NMOS source/drain regions within the semiconductor material operatively adjacent the peripheral NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the peripheral NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate, implanting conductivity-enhancing dopant into the semiconductor material to form peripheral NMOS graded junction regions operatively adjacent the peripheral NMOS transistor gate.

53. The method of claim 52 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the p-type conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

54. The method of claim 52 wherein the implanted conductivity-enhancing dopant is a p-type dopant and wherein the formed NMOS graded junction regions are halo regions.





regions operatively adjacent the peripheral NMOS transistor gate and forming memory NMOS source/drain regions operatively adjacent the memory NMOS transistor gates.

59. The method of claim 52 further comprising:

after forming halo regions operatively adjacent the NMOS source/drain regions, providing a masking layer over the peripheral NMOS region;

after providing the masking layer over the peripheral NMOS region, patterning a PMOS transistor gate over the PMOS region; and

forming electrically conductive PMOS source/drain regions operatively adjacent the PMOS transistor gate.

60. The method of claim 59 further comprising forming PMOS graded junction regions operatively adjacent the PMOS source/drain regions.

61. The method of claim 59 further comprising forming PMOS graded junction regions operatively adjacent the PMOS source/drain regions, wherein the PMOS graded junction regions are formed after the PMOS source/drain regions are formed.

62. The method of claim 59 wherein the PMOS transistor gate has opposing lateral sidewalls, and further comprising:



1 removing the overhanging capping layer from the top of the  
2 PMOS transistor gate; and

3 implanting a conductivity-enhancing dopant into the semiconductor  
4 material of the PMOS region to form PMOS graded junction regions  
5 operatively adjacent the PMOS source/drain regions.  
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FIG. 10

FIG. 10

64. A method for forming graded junction regions operatively adjacent a transistor gate, the method comprising the following steps:

providing a semiconductor material wafer;

providing a transistor gate over the semiconductor material wafer, the transistor gate comprising a layer of polysilicon and having opposing lateral sidewalls which include an exposed portion of the layer of polysilicon;

forming an oxide layer along the exposed portion of the layer of polysilicon of the lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gate and adjacent the oxide layer, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers, implanting a first conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive source/drain regions within the semiconductor material operatively adjacent the transistor gate;

after forming the electrically conductive source/drain regions, etching the sidewall spacer material adjacent the transistor gate to remove said sidewall spacers and to thereby expose the oxide layer; and

after exposing the oxide layer, implanting a second conductivity-enhancing dopant into the semiconductor material to form graded junction regions operatively adjacent the transistor gate.

1 65. The method of claim 64 further comprising, prior to forming  
2 the oxide layer along the exposed portion of the layer of polysilicon,  
3 forming graded junction regions operatively adjacent the transistor gate.  
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5 66. The method of claim 64 wherein the first conductivity-  
6 enhancing dopant is p-type, the second conductivity-enhancing dopant is  
7 n-type, and the implant of the second conductivity enhancing dopant  
8 forms halo regions.  
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10 67. The method of claim 64 wherein the first conductivity-  
11 enhancing dopant is p-type, the second conductivity-enhancing dopant is  
12 p-type, and the implant of the second conductivity enhancing dopant  
13 forms LDD regions.  
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15 68. The method of claim 64 wherein the first conductivity-  
16 enhancing dopant is n-type, the second conductivity-enhancing dopant is  
17 n-type, and the implant of the second conductivity enhancing dopant  
18 forms LDD regions.  
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20 69. The method of claim 64 wherein the first conductivity-  
21 enhancing dopant is n-type, the second conductivity-enhancing dopant is  
22 p-type, and the implant of the second conductivity enhancing dopant  
23 forms halo regions.  
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1 70. A method for forming a peripheral NMOS transistor and a  
2 memory array of NMOS transistors, the method comprising the following  
3 steps:

4 providing a semiconductor material wafer;

5 defining a memory array region, a PMOS region and a peripheral  
6 NMOS region of the wafer;

7 providing a gate layer over the PMOS, peripheral NMOS and  
8 memory array regions, the gate layer comprising a layer of polysilicon;

9 patterning the gate layer over the peripheral NMOS region to  
10 form a peripheral NMOS transistor gate, the peripheral NMOS transistor  
11 gate having opposing lateral sidewalls which include an exposed portion  
12 of the layer of polysilicon;

13 patterning the gate layer over the memory array region to form  
14 an array of memory NMOS transistor gates over the memory array  
15 region, the memory NMOS transistor gates having opposing lateral  
16 sidewalls which include an exposed portion of the layer of polysilicon;

17 while patterning the gate layer over the peripheral NMOS region,  
18 and while patterning the gate layer over the memory array regions,  
19 leaving the gate layer over the PMOS region unpatterned;

20 forming an oxide layer along the exposed portion of the layer of  
21 polysilicon of the lateral sidewalls of the peripheral NMOS transistor  
22 gate and along the exposed portions of the layer of polysilicon of the  
23 lateral sidewalls of the memory NMOS transistor gates;

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1 providing sidewall spacers adjacent the sidewalls of the peripheral  
2 and memory NMOS transistor gates and adjacent the oxide layers;

3 after providing the sidewall spacers, forming electrically conductive  
4 peripheral NMOS source/drain regions within the semiconductor material  
5 operatively adjacent the peripheral NMOS transistor gate;

6 after forming the electrically conductive NMOS source/drain  
7 regions, removing the sidewall spacers from adjacent the peripheral  
8 NMOS transistor gate; and

9 after removing the sidewall spacers, implanting conductivity-  
10 enhancing dopant into the semiconductor material to form peripheral  
11 NMOS graded junction regions operatively adjacent the peripheral NMOS  
12 transistor gate.

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14 71. The method of claim 70 further comprising, prior to forming  
15 the oxide layer along the exposed portion of the layer of polysilicon of  
16 the lateral sidewalls of the peripheral NMOS transistor gate and along  
17 the exposed portions of the layer of polysilicon of the lateral sidewalls  
18 of the memory NMOS transistor gates, providing peripheral NMOS LDD  
19 regions operatively adjacent the peripheral NMOS transistor gate and  
20 providing electrically-conductive memory array source/drain operatively  
21 adjacent the memory array transistor gates.  
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72. The method of claim 70 wherein the implant of conductivity-enhancing dopant into the semiconductor material comprises implanting p-type conductivity enhancing dopant and thereby forms peripheral NMOS halo regions operatively adjacent the peripheral NMOS transistor gate.

73. The method of claim 70 further comprising, prior to forming the oxide layer along the exposed portion of the layer of polysilicon of the lateral sidewalls of the peripheral NMOS transistor gate and along the exposed portions of the layer of polysilicon of the lateral sidewalls of the memory NMOS transistor gates, providing peripheral NMOS LDD regions operatively adjacent the peripheral NMOS transistor gate and providing electrically-conductive memory array source/drain operatively adjacent the memory array transistor gates; and wherein the implant of conductivity-enhancing dopant into the semiconductor material comprises implanting p-type conductivity enhancing dopant and thereby forms peripheral NMOS halo regions operatively adjacent the peripheral NMOS transistor gate.

74. The method of claim 70 further comprising, after providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates, and prior to forming electrically-conductive NMOS source/drain regions, providing a masking layer over the memory array region.

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75. The method of claim 70 further comprising:  
after forming peripheral NMOS graded junction regions operatively  
adjacent the NMOS source/drain regions, patterning a PMOS transistor  
gate over the PMOS region.

[illegible]

providing a semiconductor material wafer, the semiconductor wafer having a surface;

providing a transistor gate layer atop the surface of the semiconductor wafer, the transistor gate comprising an upper oxide layer and an insulative cap layer over the upper oxide layer, the upper oxide layer having an upper surface, the upper oxide upper surface being at a level above the surface of the semiconductor wafer, the insulative cap comprising an insulative cap material;

providing a masking layer over the transistor gate and over the surface of the semiconductor substrate, the masking layer having an upper surface and comprising a masking layer material;

removing masking layer material from over the transistor gate until the masking layer upper surface is about level with the level of the upper surface of the upper oxide layer; and

etching the insulative cap material to remove the insulative cap from over the transistor gate to thereby expose the upper surface of the upper oxide layer.

77. The method of claim 76 wherein the masking layer material comprises photoresist.

1 78. The method of claim 76 wherein the insulative cap material  
2 comprises silicon nitride.

3  
4 79. The method of claim 76 wherein the transistor gate  
5 comprises opposing lateral sidewalls, the method further comprising:

6 after forming the transistor gate, providing sidewall spacers  
7 adjacent the opposing lateral sidewalls of the transistor gate, the  
8 sidewalls having a top surface, the top surface of the sidewall spacers  
9 being elevationally above the upper surface of the upper oxide layer;  
10 and

11 etching the sidewall spacers to form flat top surfaces of the  
12 sidewall spacers, the flat top surfaces being elevationally at about the  
13 same level as the exposed upper surface of the upper oxide layer of  
14 the transistor gate.  
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1 80. The method of claim 76 wherein the transistor gate  
2 comprises opposing lateral sidewalls, the method further comprising:

3 after forming the transistor gate, providing sidewall spacers  
4 adjacent the opposing lateral sidewalls of the transistor gate, the  
5 sidewalls having a top surface, the top surface of the sidewall spacers  
6 being elevationally above the upper surface of the upper oxide layer,  
7 the sidewall spacers comprising a sidewall spacer material which is  
8 identical to the material of the insulative cap; and

9 etching the sidewall spacer material to form flat top surfaces of  
10 the sidewall spacers, the flat top surfaces being elevationally at about  
11 the same level as the exposed upper surface of the upper oxide layer  
12 of the transistor gate, the etching of the sidewall spacer material  
13 occurring concurrently with the etching of the insulative cap material.

14  
15 81. The method of claim 80 wherein the insulative cap material  
16 and the sidewall spacer material both comprise silicon nitride.  
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82. A method for forming CMOS circuitry, the method comprising the following steps:

providing a semiconductor material wafer, the semiconductor wafer having a surface;

defining a PMOS region and an NMOS region of the wafer;

providing a gate layer over the PMOS region and over the NMOS region, the gate layer having an upper oxide layer and an insulative cap over the upper oxide layer, the upper oxide layer having an upper surface, the upper oxide upper surface being at a level above the surface of the semiconductor wafer, the insulative cap comprising an insulative cap material;

patterning the gate layer over the NMOS region to form an NMOS transistor gate over the NMOS region while leaving the gate layer over the PMOS region unpatterned;

providing a masking layer over the PMOS region and the NMOS region, the masking layer having an upper surface and comprising a masking layer material;

removing masking layer material from over the PMOS and NMOS regions until the masking layer upper surface is about level with the level of the upper surface of the upper oxide layer; and

etching the insulative cap material to remove the insulative cap from over the NMOS gate and from over the unpatterned gate layer over the PMOS region to thereby expose the upper surface of the upper oxide layer of the NMOS gate and to also thereby expose the

1 upper surface of the upper oxide layer of the unpatterned gate layer  
2 over the PMOS region.

3  
4 83. The method of claim 82 wherein the masking layer material  
5 comprises photoresist.

6  
7 84. The method of claim 82 wherein the insulative cap material  
8 comprises silicon nitride.

9  
10 85. The method of claim 82 wherein the NMOS transistor gate  
11 comprises opposing lateral sidewalls, the method further comprising:

12 after forming the NMOS transistor gate, providing sidewall spacers  
13 adjacent the opposing lateral sidewalls of the NMOS transistor gate, the  
14 sidewalls having a top surface, the top surface of the sidewall spacers  
15 being elevationally above the upper surface of the upper oxide layer;  
16 and

17 etching the sidewall spacers to form flat top surfaces of the  
18 sidewall spacers, the flat top surfaces being elevationally at about the  
19 same level as the exposed upper surface of the upper oxide layer of  
20 the NMOS gate.

1 86. The method of claim 82 wherein the NMOS transistor gate  
2 comprises opposing lateral sidewalls, the method further comprising:

3 after forming the NMOS transistor gate, providing sidewall spacers  
4 adjacent the opposing lateral sidewalls of the NMOS transistor gate, the  
5 sidewalls having a top surface, the top surface of the sidewall spacers  
6 being elevationally above the upper surface of the upper oxide layer,  
7 the sidewall spacers comprising a sidewall spacer material which is  
8 identical to the material of the insulative cap; and

9 etching the sidewall spacer material to form flat top surfaces of  
10 the sidewall spacers, the flat top surfaces being elevationally at about  
11 the same level as the exposed upper surface of the upper oxide layer  
12 of the NMOS gate, the etching of the sidewall spacer material occurring  
13 concurrently with the etching of the insulative cap material.  
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15 87. The method of claim 86 wherein the insulative cap material  
16 and the sidewall spacer material both comprise silicon nitride.  
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1 88. A method for forming an NMOS transistor device and an  
2 insulated word line, the method comprising the following steps:

3 providing a semiconductor material wafer, the semiconductor wafer  
4 having a surface;

5 defining a memory array region of the wafer and a peripheral  
6 NMOS region of the wafer;

7 providing a gate layer over the peripheral NMOS and memory  
8 array regions of the wafer, the gate layer having an upper oxide layer  
9 and an insulative cap over the upper oxide layer, the upper oxide layer  
10 having an upper surface, the upper oxide layer upper surface being at  
11 a level above the surface of the semiconductor wafer, the insulative cap  
12 comprising an insulative cap material;

13 patterning the gate layer over the peripheral NMOS region to  
14 form a peripheral NMOS transistor gate over the peripheral NMOS  
15 region, the peripheral NMOS transistor gate having opposing lateral  
16 sidewalls;

17 patterning the gate layer over the memory array region to form  
18 a word line, the word line having opposing lateral sidewalls;

19 providing insulative sidewall spacers adjacent the opposing lateral  
20 sidewalls of the peripheral NMOS transistor gate and adjacent the  
21 opposing lateral sidewalls of the word line, the sidewall spacers  
22 comprising a sidewall spacer material;

23  
24

1 providing a masking layer over the peripheral NMOS region, the  
2 masking layer having an upper surface and comprising a masking layer  
3 material;

4 removing the masking layer material from over peripheral NMOS  
5 region until the masking layer upper surface is about level with the  
6 upper oxide layer upper surface; and

7 removing the insulative cap material from over the peripheral  
8 NMOS transistor gate to expose the upper oxide upper surface of the  
9 peripheral NMOS gate.

10  
11 89. The method of claim 88 further comprising:

12 prior to removing the masking layer material from over the  
13 peripheral NMOS transistor gate, providing a masking layer over the  
14 word line, the masking layer over the word line comprising a masking  
15 layer material identical to the masking material of the masking layer  
16 over the peripheral NMOS transistor gate, the masking layer material  
17 over the word line having an upper surface which is elevationally above  
18 the upper surface of the masking material over the peripheral NMOS  
19 transistor gate; and

20 wherein the step of removing the masking layer material from  
21 over peripheral NMOS region leaves masking layer material over the  
22 word line.  
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1 90. The method of claim 88 further comprising:  
2 prior to removing the insulative cap from over the peripheral  
3 NMOS transistor gate, providing a masking layer over the word line.

4  
5 91. The method of claim 88 further comprising:  
6 defining a PMOS region of the semiconductor material wafer;  
7 providing the gate layer over the PMOS region;  
8 while patterning the gate layer over the peripheral NMOS region,  
9 and while patterning the gate layer over the memory array region,  
10 leaving the gate layer over the PMOS region unpatterned; and  
11 while providing the masking layer over the peripheral NMOS  
12 region, also providing the masking layer over the PMOS region.  
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92. The method of claim 88 further comprising:  
defining a PMOS region of the semiconductor material wafer;  
providing the gate layer over the PMOS region;  
while patterning the gate layer over the peripheral NMOS region,  
and while patterning the gate layer over the memory array region,  
leaving the gate layer over the PMOS region unpatterned;  
while providing the masking layer over the peripheral NMOS  
region, also providing the masking layer over the PMOS region;  
wherein the step of removing the masking layer material from  
over peripheral NMOS region also removes masking layer material from  
over the PMOS region; and  
wherein the step of removing the insulative cap material from  
over the peripheral NMOS transistor gate to expose the upper oxide  
upper surface of the peripheral NMOS gate also removes insulative cap  
material from over the PMOS region to expose an upper oxide surface  
of the unpatterned masking material over the PMOS region.

1           93. The method of claim 88 wherein the sidewall spacers of the  
2 peripheral NMOS transistor have a top surface, the top surfaces of the  
3 sidewall spacers being elevationally above the upper surface of the  
4 upper oxide layer of the peripheral NMOS transistor, the method  
5 further comprising:

6           etching the sidewall spacers of the peripheral NMOS transistor to  
7 form flat top surfaces of the sidewall spacers of the peripheral NMOS  
8 transistor, the flat top surfaces being elevationally at about the same  
9 level as the exposed upper surface of the upper oxide layer of the  
10 peripheral NMOS gate.  
11

12           94. The method of claim 88 wherein the sidewall spacers of the  
13 peripheral NMOS transistor have a top surface, the top surfaces of the  
14 sidewall spacers being elevationally above the upper surface of the  
15 upper oxide layer of the peripheral NMOS transistor, the method  
16 further comprising:

17           etching the sidewall spacer material of the peripheral NMOS  
18 transistor to form flat top surfaces of the sidewall spacers of the  
19 peripheral NMOS transistor, the flat top surfaces being elevationally at  
20 about the same level as the exposed upper surface of the upper oxide  
21 layer of the peripheral NMOS gate, the etching of the sidewall spacer  
22 material occurring concurrently with the etching of the insulative cap  
23 material.  
24

1 95. The method of claim 88 further comprising patterning the  
2 gate layer over the memory array region to form memory transistor  
3 gates.

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5 96. The method of claim 88 wherein the insulative cap material  
6 and the sidewall spacer material both comprise silicon nitride.  
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FIG. 10

97. A method for forming a PMOS transistor device, a peripheral NMOS transistor device, and one or more memory NMOS transistor devices, the method comprising the following steps:

providing a semiconductor material wafer;

defining a PMOS region, a peripheral NMOS region, and a memory array region of the wafer;

providing a gate layer over the PMOS, peripheral NMOS and memory array regions;

patterning the gate layer over the peripheral NMOS region to form a peripheral NMOS transistor gate;

patterning the gate layer over the memory array region to form one or more memory array transistor gates;

while patterning the gate layer over the peripheral NMOS and memory array regions, leaving the gate layer over the PMOS region unpatterned;

forming source/drain regions, halo regions and LDD regions operatively adjacent the peripheral NMOS transistor gate, and forming source/drain regions operatively adjacent the one or more memory NMOS transistor gates, the steps of forming the regions occurring in a sequence such that one or more of the regions are formed last and are therefore last formed regions; and

less than two masking layer provision steps after the formation of the peripheral NMOS transistor gate, and prior to the formation of the one or more last formed regions.

1 98. A method of forming a transistor structure on a  
2 semiconductor substrate, comprising the following steps:

3 providing a transistor gate assembly formed on said substrate, said  
4 gate assembly including sidewall spacers extending to said substrate;

5 doping a first region of said substrate with a selected dopant;

6 removing a lateral portion of at least one of said sidewall spacers,  
7 while leaving a part of said at least one of said sidewall spacers in  
8 place; and

9 after said removal, doping a second portion of said substrate.  
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